SBC 7000 DSP-LC FPGA Upgrade

Method of Procedure

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1 Introduction

1.1 Overview

This Method of Procedure (MOP) is intended to provide detailed instructions for upgrading the SBC 7000 DSP-LC FPGA from the BMC GUI.

1.2 Target Platform

This Method of Procedure (MOP) is intended only for upgrading the FPGA image of an SBC 7000 DSP-LC card.

1.3 Target Firmware and FPGA Version

This Method of Procedure (MOP) is intended to be used only for upgrading the FPGA image of an SBC 7000 DSP-LC card when the system is running firmware version 1.25.0, and the DSP-LC card has an FPGA image version that is older than 2014/06/11. To verify the FPGA version, refer to section 2 “How to Verify FPGA Version” for guidance.

2 How to Verify FPGA Version

Run the following command to verify the FPGA version:

1. Execute the steps in section 3.2 “Preparing BMC for FPGA Programming Utility”.
2. dsppldprogrammer –s[2,3,4,5] –t3 –aVERSION where –s[2,3,4,5] is the required slot number. This command displays current programmed flash fpga version.

   Sample Output:

   #dsppldprogrammer –s2 –t3 –aVERSION
   JAM STAPL ByteCode Player Version 2.2
   Copyright © 1998-2001 Altera Corporation

   LOADING DSP100 FPGA Header From SPI Flash…

   ==========
   FPGA SPI FLASH VERSION INFORMATION SLOT 0
   ==========

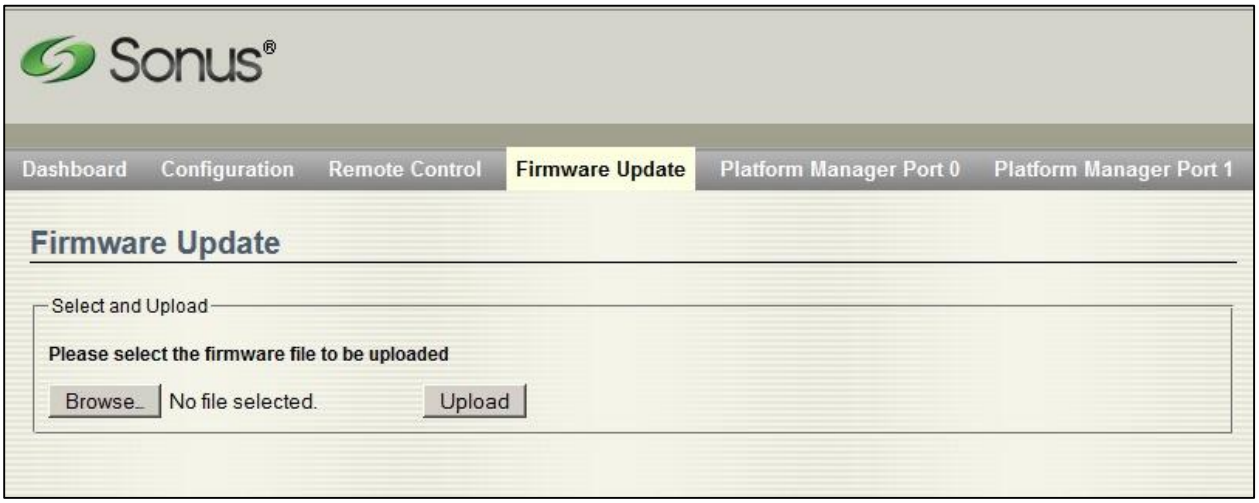
   Design Name: sps_fic2;UserID=0XFFFFFFFF
   Device Name: 7vx415tffg1158
   Version: 2014/06/11 16:34:07
   Image Length: 0x009b60cc
   ==========
3. Reboot the BMC.

3 Procedure

3.1 Uploading DSP-LC file in BMC Web GUI

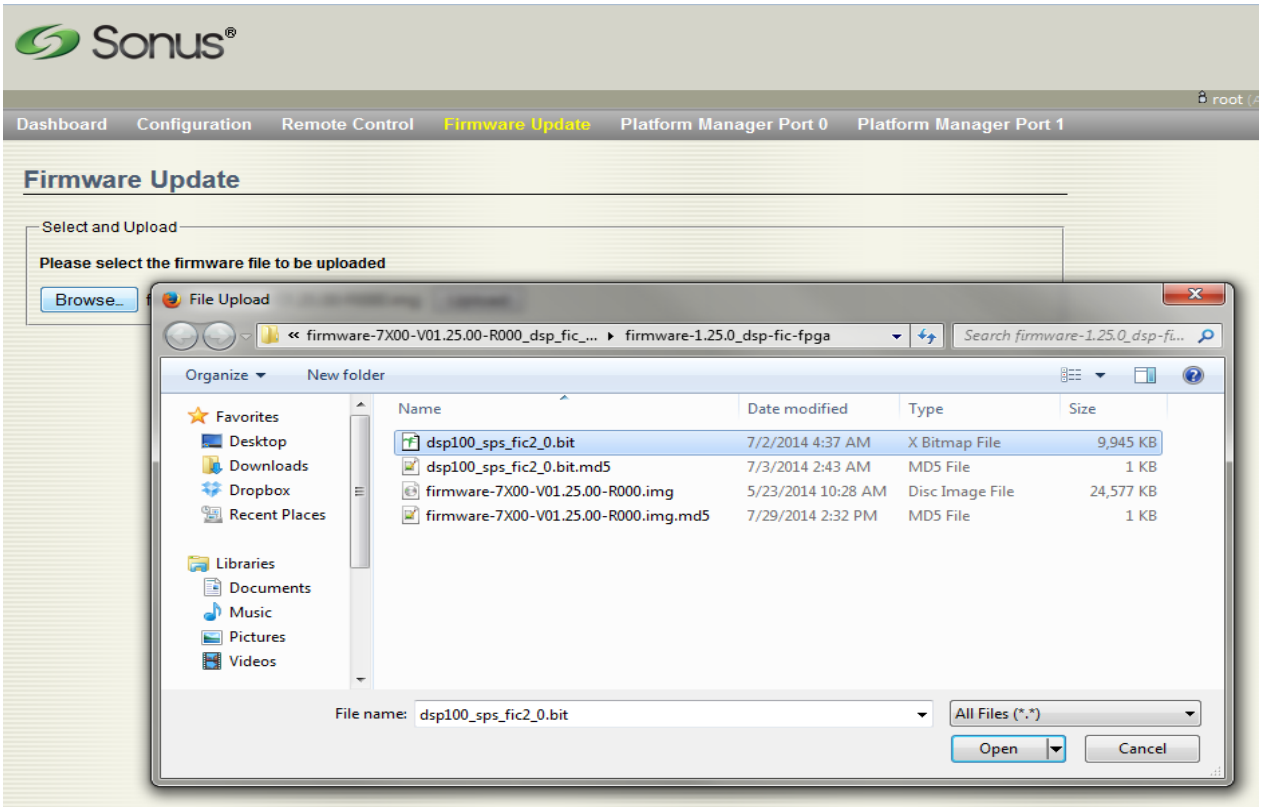
1. Untar/Extract the SBC 7000 firmware “***firmware-7X00-V01.25.00-R000_dsp_fic_fpga_20140611.tar.gz”.*** The tar file contains *firmware-7X00-V01.25.00-R000.img* and *dsp100_sps_fic2_0.bit* and associated .md5 files.
2. Login to BMC Web GUI.
3. Verify the BMC Version in the **Dashboard** (home screen) page. Make sure the BMC version is 1.25.0.
4. Click **Firmware Update** tab.

Figure 1 Firmware Update Tab



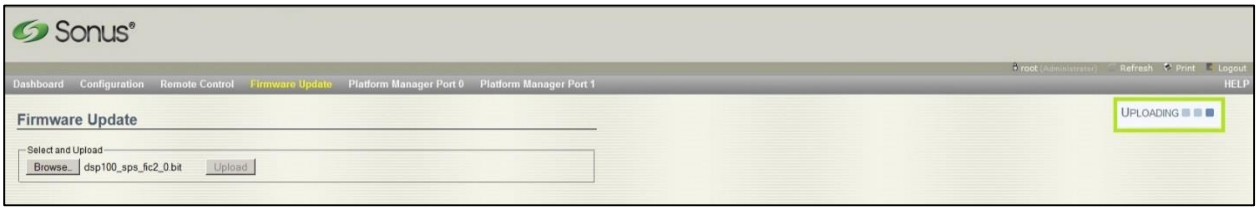
5. Click **Browse** and select FPGA package file.

Figure 2 Browsing FPGA Package



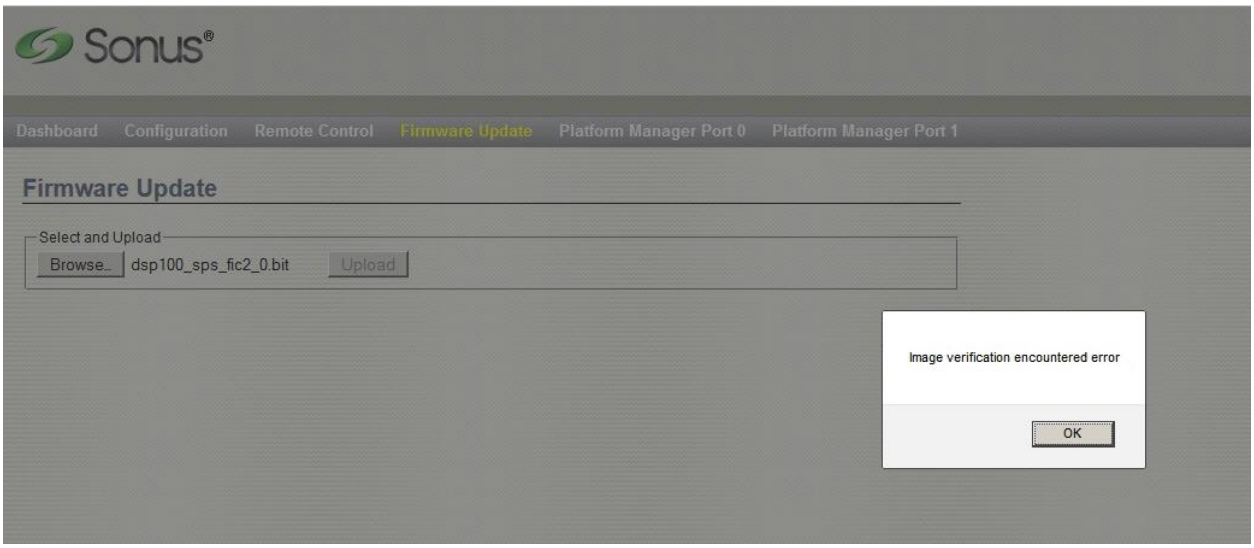
6. Click **Upload**. This will take several minutes to upload.

Figure 3 Uploading FPGA Package



7. After upload is completed, an "image verification encountered error" message appears. Click **OK** to ignore this error.

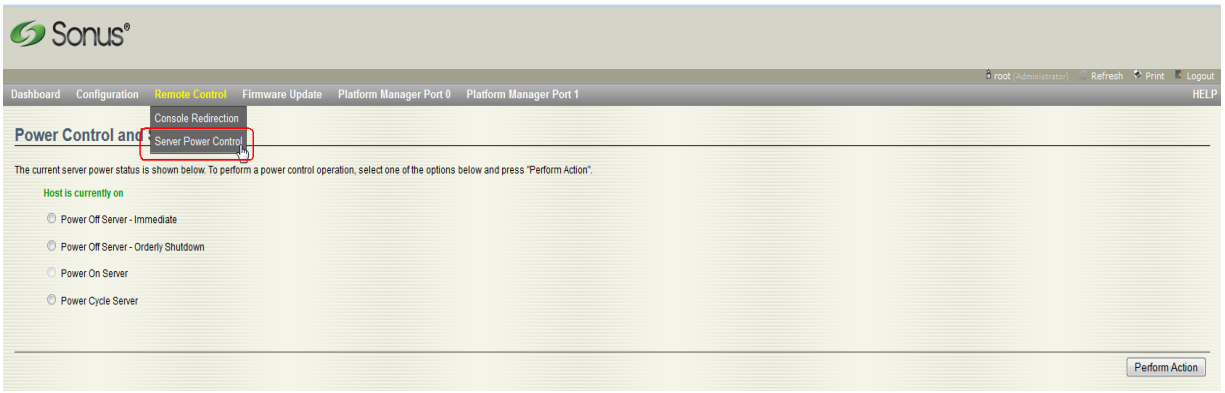
Figure 4 Ignoring Image Verification Error Message



3.2 Preparing BMC for FPGA Programming Utility

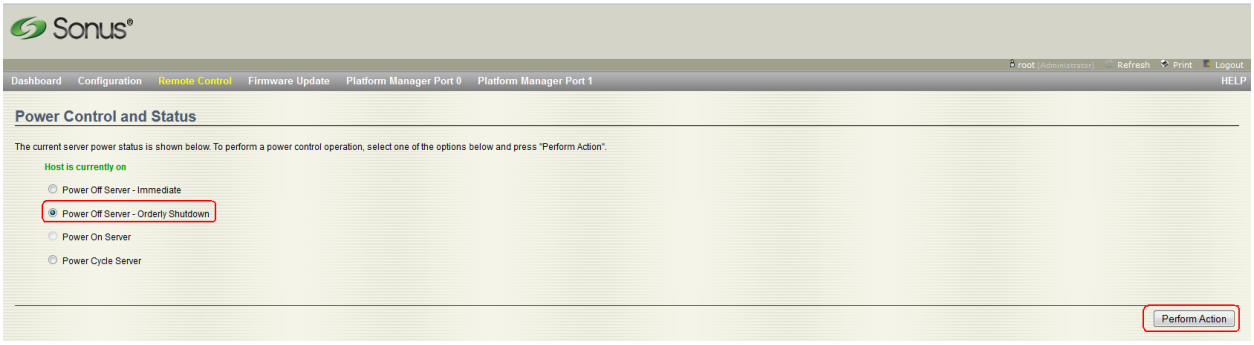
1. Login to BMC GUI.
2. Click **Remote Control > Server Power Control** tab.

Figure 5 Server Power Control Tab



3. Select **Power Off Server – Orderly Shutdown** and click **Perform Action**.

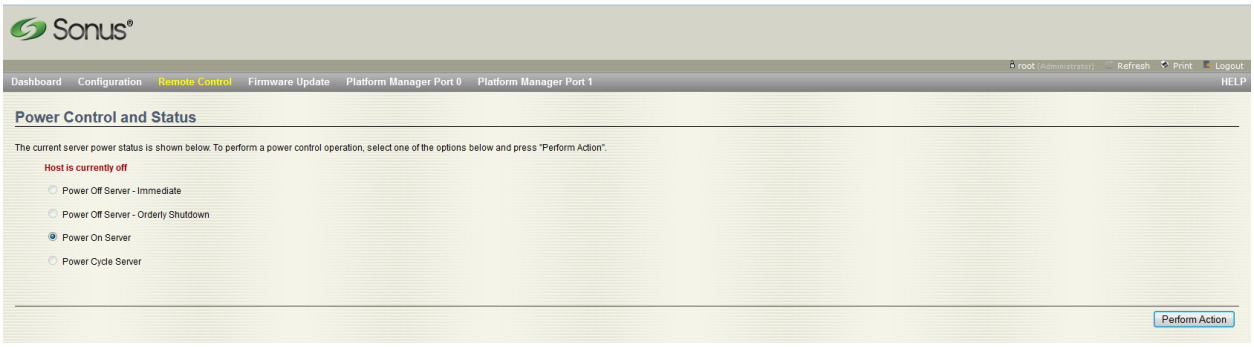
Figure 6 Orderly Shutdown of Host



Note: This performs a graceful shutdown of the host and may take a few minutes.

4. Confirm the **Power off** status.

Figure 7 Power Off Status



5. Login to BMC through ssh.
6. Stop the IPMI run using the following command:
    - /etc/init.d/ipmistack stop

3.3 Programming FPGA Utility

1. Login to BMC through ssh.
2. Run the following commands to program FPGA utility:
    a. cd /var
    b. cp upgrade/fw.img ./dsp100fpga.rom
    c. dsppldprogrammer –s[2,3,4,5] –t3 –aPROGRAM dsp100fpga.rom
        where -s[2,3,4,5] choose required slot number.

    This takes around 15-20 minutes to complete.

    Sample Output:

    #dsppldprogrammer –s2 –t3 –aPROGRAM dsp100fpga.rom
    JAM STAPL ByteCode Player Version 2.2
    Copyright © 1998-2001 Altera Corporation

    Loading DSP100 FPGA Image from File [dsp100fpga.rom] to memory…COMPLETE
    Erasing DSP100 SPI Flash [Slot 0]…COMPLETE

    *Programming DSP100 SPI Flash [Slot 0]…*********-> COMPLETE*

    #

3. OPTIONAL verify. Execute the steps listed in verify block section if you want to verify.
4. Repeat steps 1 to 2 to program more DSP slots
5. Reboot the BMC after completion.

3.3.1 Verify Block (Optional)

1. Run the following command to verify the programming
   a. dsppldprogrammer –s[2,3,4,5] -t3 –aVERIFY

      where –s[2,3,4,5] is the required slot number.

      Sample Output:

      # dsppldprogrammer –s2 –t3 –aVERIFY
      JAM STAPL ByteCode Player Version 2.2
      Copyright © 1998-2001 Altera Corporation

      Loading DSP100 FPGA Image from SPI Flash [Slot = 0] ...COMPLETE

      #

      This takes around 20 minutes. This saves dsp100FpgaSlot_x.rom in **/var**

      where x =[0,1,2,3].

   b. # dd if=dsp100fpga.rom of=dsp100fpga_cmp.rom bs=4 count=2545738

      2545738+0 records in
      2545738+0 records out

      This command must be run only once and it takes about a minute to complete.

   c. # diff dsp100fpga_cmp.rom dsp100FpgaSlot_x.rom

      where x = [0,1,2,3] depending on the slot number of the DSP.

      #

      The successful ***diff*** command provides no output.
2. Reboot the BMC.